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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/747,928	12/27/2000	Byung-Young Ahn	3430-0140P	3449

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BIRCH STEWART KOLASCH & BIRCH  
PO BOX 747  
FALLS CHURCH, VA 22040-0747

EXAMINER
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TRAN, BINH X

ART UNIT	PAPER NUMBER
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1765

DATE MAILED: 05/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

**Application No.**

09/747,928

**Applicant(s)**

AHN, BYUNG-YOUNG

**Examiner**

Binh X Tran

**Art Unit**

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 26 February 2004.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 7-17, 19 and 20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 7-17, 19 and 20 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

## DETAILED ACTION

### ***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 17, 19, 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dhindsa et al. (US 5,904,779) in view of Kanno et al. (US 6,243,251).

Dhindsa discloses a method of processing a substrate comprising:

providing an electrode plate (206);

providing an intermediate material (210) on the surface of the electrode plate (206);

before lifting the pin positioning a substrate (208) at a predetermined distance from the electrode plate using thickness of the insulate film (210) to obtain an intermediate structure (Fig 2B, Note: the examiner interpret the thickness of the insulating layer 210 read on "a predetermined distance from the electrode plate")

processing the intermediate structure;

removing the substrate from the electrode plate (abstract).

Dhindsa further discloses that the sticking force (read on "electrostatic attraction between the substrate and the electrode plate") is depending on the distance and it is produced by electrostatic chuck (206). The electrode static chuck has an insulating

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material (210) over it to insulate the chuck from the substrate. The thickness of the insulating layer (210) creates a space/distance between the substrate and the electrode (i.e., electrostatic chuck 206). Therefore, before lifting the pins, this distance (the thickness of layer 210) certainly reduce electrostatic force in comparison without having this distance.

Dhindsa fails to disclose that the insulating material (210) is insulating vacuum tape. In a semiconductor method, Kanno discloses the use of insulating vacuum adhesive/tape layer (36) (read on "insulating tape") on the electrostatic chuck to reduce residual attraction force (abstract, col. 17 lines 55 to col. 18). Kanno further discloses the attracting force is reduced as the thickness of the spacer increased. It would have been obvious to one having ordinary skill in the art, at the time of invention, to modify Dhindsa in view of Kanno by using the insulating vacuum tape layer because it will help to reduce attracting force.

Kanno does not explicitly disclose the insulating vacuum tape have characteristics which do not lower a degree of vacuum. However, Kanno and the present invention use the same material (i.e. insulating vacuum tape/adhesive). According to the MPEP 2112.01, "The product of identical chemical composition cannot have mutual exclusive property. Chemical composition and its properties are inseparable". Therefore, if the prior art teaches the identical chemical composition, the properties applicant discloses and/or claims (i.e., have characteristics which do not lower a degree of vacuum) are necessarily present.

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Respect to claim 19, Dhindsa teaches the step of positioned the substrate at the predetermined position from the electrode plate (206) by placing an intermediate material (210) between the substrate (208) and electrode plate (Fig 2A, col. 4 lines 6-15).

Respect to claim 20, Dhindsa further teaches the step of:

- providing an electrode;
- providing an intermediate material (210) on the electrode (Fig 2A);
- providing a substrate on the intermediate material (210) of the electrode to obtain an intermediate structure and processing the intermediate structure (Fig 2A);
- processing the intermediate structure;
- removing the substrate from the electrode using a plurality of pins (218) formed on the electrode to push the substrate away from the electrode (Fig 3-5). All other limitations in claim 20 have been discussed above.

3. Claims 7-10, 12, 14-16 are rejected under 35 U.S.C 103(a) as being unpatentable over Dhindsa in view of Kanno (US 6,243,251) and further in view of Nakamura (US 6,096,572)

Respect to claim 7, Dhindsa discloses a method comprising an apparatus having:

- a process chamber having a gas inlet, the gas inlet allowing a reactive gas (i.e., plasma) into the process chamber;
- a first electrode arranged at a predetermined location in the process chamber (col. 4 lines 1-2);

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a second electrode (206) in the chamber spaced apart from and opposite to the first electrode, having insulating film (210), a plurality of lift pins (218) received in a plurality of hole, the insulating material (210) being arranged between the plurality of lifts pin (See Fig 2a-2c);

a power source (RF source, see col. 4 lines 2, and electrical connecting arrangement (224) for applying voltage to the first and second electrode;

arranging the substrate (208) on the second electrode (206);

dry etching the substrate (col. 3 lines 60-67);

separating the substrate from the second electrode (206) using the lift pins (218) (See Fig 2-6).

The limitation regarding 'reduces an electrostatic attraction between the second electrode and substrate prior to a lifting of the substrate' has been discussed above. Dhindsa fails to disclose that the insulating material (210) is insulating tape. In a semiconductor method, Kanno discloses the use of insulating vacuum adhesive/tape layer (36) on the electrostatic chuck to reduce residual attraction force (abstract, col. 17 lines 55 to col. 18). Kanno further discloses the attracting force is reduced as the thickness of the spacer increased. It would have been obvious to one having ordinary skill in the art, at the time of invention, to modify Dhindsa in view of Kanno by using the adhesive layer because it will help to reduce attracting force.

Kanno does not explicitly disclose the vacuum insulating tape have characteristics which do not lower a degree of vacuum. However, Kanno and the present invention use the same material (i.e. vacuum insulating tape). According to the

MPEP 2112.01, "The product of identical chemical composition cannot have mutual exclusive property. Chemical composition and its properties are inseparable".

Therefore, if the prior art teaches the identical chemical composition, the properties applicant discloses and/or claims (i.e., have characteristics which do not lower a degree of vacuum) are necessarily present.

Both Dhindsa and Kanno do not explicitly use the term "array substrate" in their invention. Nakamura teaches the substrate can be array substrate. It would have been obvious to one having ordinary skill in the art, at the time of invention, to modify Dhindsa and Kanno in view of Nakamura by using array substrate because equivalent and substitution of one for the other would produce an expected result.

Respect to claim 8, both Dhindsa and Kanno teaches the process chamber is a vacuum chamber. Respect to claim 9, Kanno teaches adhesive layer (36) is used in the vacuum chamber. The examiner interprets that Kanno's adhesive layer in the vacuum chamber read on the limitation of "vacuum tape". Respect to claim 10, both Dhindsa and Kanno teaches the power source generates RF power (Dhindsa col. 4 lines 1-2; Kanno col. 10 lines 13-25).

Respect to claims 12 and 14, Dhindsa teaches that the dry etching process is a plasma and/or reactive ion etching. The limitations of claims 15-16 have been discussed in previous paragraphs.

4. Claim 11 is rejected under 35 U.S.C 103(a) as being unpatentable over Dhindsa, Kanno and Nakamura as applied to claim 7 above, and further in view of Collins et al. (US 5,874,361).

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Respect to claim 11, Kanno teaches a DC power source (8a/8b) for applying a DC voltage to the lower electrode. Kanno fails to teach applying DC voltages to both electrodes. Collins teaches applying DC voltage to upper and lower electrodes (Fig 1). It would have been obvious to one having ordinary skill in the art, at the time of invention, to modify Dhindsa, Kanno, and Nakamura in view of Collins by applying DC voltages to both electrodes because it would produce uniform high density plasma.

5. Claim 13 is rejected under 35 U.S.C 103(a) as being unpatentable over Dhindsa, Kanno and Nakamura as applied to claim 7 above, and further in view of Westwood (US 5,985,104)

Respect to claim 13, Dhindsa does teach that the dry etching is an ion beam milling etching. However, Dhindsa clearly teaches the dry etching process is RIE. In a semiconductor process, Westwood teaches that RIE can be used instead of ion beam milling. It would have been obvious to one having ordinary skill in the art, at the time of invention, to modify Dhindsa, Kanno, Nakamura in view of Westwood by using ion beam milling because equivalent and substitution of one for the other would produce an expected result.

### ***Response to Arguments***

6. Applicant's arguments filed 2-26-2004 have been fully considered but they are not persuasive.

Applicants argue that the thickness of the insulating layer (210) "may be taken in consideration as an afterthought (hindsight), neither the thickness of the thickness of the insulating layer 210 or the distance between the array substrate and the second



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electrode is taken into consideration ... for the purpose of reducing an electrostatic force attraction between the second electrode and the array substrate". The examiner disagrees. Dhindsa clearly teaches that the thickness of the insulating layer (the distance between the array substrate and the second electrode) always exists under any circumstance. The array substrate will always have at least this distance to separate with the second electrode. The examiner does not suggest modifying this thickness or distance as an afterthought or hindsight as stated by Applicants. Further, Dhindsa clearly teaches the insulating layer is used for electrically isolating the chuck/electrode from the substrate. Therefore, before lifting the substrate, the thickness of the insulating layer will help to reduce the sticking force (i.e. electro static force).

The Applicants further argue that contra to applicant's invention "Dhindsa discloses that the sticking force increases when the substrate is lift, i.e., when the distance is increased (Col. 6 lines 14-35)". This argument is not commensurate with the scope of the claim. Applicants did not claim any relationship between the "sticking force" (i.e. electro static force) and the distance when the substrate is lifted or any time afterward.

Applicants further argue that layer (36) of Kanno is "conventional adhesive" and it is different from the Applicant's vacuum insulating tape. According to Applicants, "The layer 36 of Kanno, cited by the examiner, is an adhesive layer, and as such, inherently lowers a degree of vacuum". The examiner disagrees. Applicants did not disclose the chemical composition of the insulating tape. Applicants only disclose that the insulating tape is a vacuum tape (page 4line 26-27). Kanno clearly discloses the layer 36 is a

vacuum tape (the same generic material with applicants) and it is used in a vacuum chamber. Applicants never define what is the specific kind of material/composition can be consider as "conventional" adhesive/tape. Therefore, the examiner still maintain that Kanno is a proper prior art under the U.S.C § 103.

***Conclusion***

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Binh X Tran whose telephone number is (571) 272-1469. The examiner can normally be reached on Monday-Thursday and every other Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine G Norton can be reached on (571) 272-1465. The fax phone

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number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Binh X. Tran

**NADINE G. NORTON**  
**SUPERVISORY PATENT EXAMINER**

